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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/340,776	06/28/1999	GAJINDER SINGH PANESAR	S1022/8250	4340

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05/05/2003

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EXAMINER

PHAN, THAI Q

ART UNIT

PAPER NUMBER

2123

DATE MAILED: 05/05/2003

21

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/340,776

Applicant(s)

Gajinder Singh Panesar

Examiner

Thai Phan

Art Unit

2123

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Feb 19, 2003
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-5 is/are allowed.
- 6) ☒ Claim(s) 6 and 7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on Aug. 16, 1999 is/are a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 14, 20 6) ☐ Other:

DETAILED ACTION

This Office Action is in response to applicant's RCE filed on Feb. 19, 2003. Claims 1-7 are pending in this official action.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The formal drawing, filed on Aug. 16, 1999 have been received and entered.

Information Disclosure Statement

3. The information disclosure statements filed 01/27/2003 and 03/04/2003 have been considered and placed in the record.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aleksic et al., US Patent no. 5,995,736.

As per claim 6, Aleksic discloses method and system for simulating integrated circuit including ASIC design or application specific processor (ASP) substantially similar to the claimed invention (Abstract and Summary of the Invention). According to Aleksic, the simulation system includes means for defining functional model for the processor (col. 2, lines 45-56, col. 4, line 1-53, col. 5, lines 18-31), means for simulating functional model based on hardware design and outputting result of simulation, means for converting result of hdl functional model simulation into a simulation language such as C/C++, for instance (col. 5, line 8 to col. 6, line 6, line 56) and means for simulating the circuit design at circuit level (col. 5, lines 37-67, col. 7, lines 40-60, col. 8, lines 8-60). Aleksic does not expressly disclose subsequent phase for simulating the loaded modeling files as claimed.

Practitioner in the art at the time of the invention was made could have found Aleksic disclosure of extract register information in .REG file (col. 5, lines 31-36), the register generator (36) generating register files for hardware design simulation code (38) in col. 6, line 48-55 col. 7, lines 3-17, and connection files as in col. 7, lines 41-60 would be used for generation of hardware design simulation codes (col. 11, lines 42-50) for subsequent phase of simulation of loaded modeling files because such simulation information is extracted and connected to become available for subsequent simulation at the circuit level for those skilled in the art to utilize such useful available resources.

As per claim 7, claim 7 is directed to computer program product for performing steps for the system claim 6 above, and Aleksic discloses computer program product including modeling file as claimed (Abstract and Summary of the Invention). According to Aleksic, the simulation system includes program product means for defining functional model for the processor (col. 4, line 30-65), a program product for simulating functional model based on hardware design (col. 2, lines 45-56, col. 4, lines 30-65, col. 5, lines 18-31), programming means for generating interface function file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface for subsequent circuit level simulation (col. 5, lines 55-67, col. 7, lines 40-60), program means for simulating in the high level language as part of the functional model an application executable by the CPU, including for a predetermined simulation phase, test function files, and operation of the set of peripheral devices, outputting the state of the application and the state of the peripherals to the modeling file for converting the modeling file in the high level programming language to a language executable by the simulation system (Figs. 2-4, col. 4, lines 48-65, col. 5, lines 18-31, col. 6, lines 15-35, cols. 7-8), means for converting result of hdl functional model simulation into a simulation language such as C/C++ for instance (col. 5, line 8 to col. 6, line 56), and means for simulating the application specific integrated circuit design as claimed. Aleksic does not expressly disclose simulating the loaded modeling files for a subsequent simulation phase as claimed.

Practitioner in the art at the time of the invention was made could have found Aleksic disclosure of extract register information in .REG file (col. 5, lines 31-36), the register generator

(36) generating register files for hardware design simulation code (38) in col. 6, line 48-55 col. 7, lines 3-17, and connection files as in col. 7, lines 41-60 would be used for generation of hardware design simulation codes (col. 11, lines 42-50) for subsequent phase of simulation of loaded modeling files. In other words, the state information available from the functional model simulation could be used for subsequent simulation phase in the circuit level to verify the specific processor performance in the system.

Allowable Subject Matter

6. Claims 1-5 are allowed. The following is an examiner's statement of reasons for allowance: the claimed invention is method and system for simulating integrated circuit including ASIC design or application specific processor (ASP). The simulation system includes means and functional steps for defining functional model for the processor, means for simulating functional model based on hardware design, generating interface function file for hardware interface which defines the communication of the peripheral with the processor, simulating in the high level language as part of the functional model an application executable by the CPU, including for a predetermined simulation phase, test function files, and operation of the set of peripheral devices, outputting the state of the application and the state of the peripherals at the end of a predetermined simulation phase to a modeling file in the high level language and converting the modeling file in the high level programming language to a language executable by the simulation system, means for converting result of hdl functional model simulation into a simulation language for simulating , and means for simulating the application specific integrated

circuit design as claimed. The art of record does not expressly disclose such feature limitations as in claims 1-5.

Response to Arguments

7. Applicant's arguments filed on Feb. 19, 2003 have been fully considered but they are moot in view of a new ground of rejection.

In response to applicant's remark Aleksic fails to disclose or suggest means for simulating an ASP in which the state of the functional model at the end of a simulation phase is used to simulate the ASP at circuit level (page 3, last paragraph to page 4, paragraph 1), the examiner responds such argued features are obvious in Alexic disclosure. It's obvious for those skilled in the related art because based upon Aleksic disclosure of extract register information in .REG file (col. 5, lines 31-36), the register generator (36) generating register files for possibly subsequent hardware design simulation code (38) in col. 6, line 48-55 col. 7, lines 3-17, and connection files as in col. 7, lines 41-60 would be used for generation of hardware design simulation codes (col. 11, lines 42-50) for subsequent phase of simulation of loaded modeling files. In other words, ASP simulation files have been used for subsequent simulation or emulation at the circuit level for simulation of peripheral devices for example as claimed to verify the whole system performance.

In response to applicant's argument Aleksic fails to disclose or suggest using state of the simulation of the functional model to simulate the ASP at the circuit level in a subsequent simulation phase (page 4, last paragraph), the examiner disagrees with. Alexic discloses functional model and its states has been used to simulate the ASP could be used for subsequent

simulation phase at the circuit level such simulation phase could use state of the simulation of the functional model for simulation of the ASIC at the circuit level (col. 5, lines 55-67), or circuit level in a subsequent simulation phase as in applicant's argument, to verify circuit performance.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

May 4, 2003

Thai Phan
Patent Examiner
AV 2123